AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims

1-12. (Cancelled)

13. (New) A Processing Unit (PA) for processing a plurality of data streams by an algorithm divided into a plurality of process steps, said PA comprising:

an interconnection unit comprising means for switching;

Process Step (PS) means comprising at least two PS modules, where each PS module is connected to the interconnection unit and a scheduler connected to said interconnection unit and to each PS module;:

a memory unit comprising at least two memories wherein each memory is connected to the interconnection unit;

the interconnection unit further comprising means for providing at least a first connection between one of said memories and one of said PS modules and a second connection between another of said memories and another of said PS modules, wherein the interconnection unit is adapted to connect each memory to each of the PS modules by a switching activity, wherein the switching activity and the processing of the PS modules are controlled by the scheduler; and

each memory comprises means for storing a data stream and said stored data streams are manipulated in parallel by the connected PS modules respectively, during a predetermined time period between said switching activities.

14. (New) The Processing Unit (PA) according to claim 13, further comprising at least one external memory for storing at least input and output data for the memories within the memory unit.

15. (New) The Processing Unit (PA) according to claim 13, wherein said data streams are channels in a communication system.

16. (New) The Processing Unit (PA) according to claim 13, wherein said channels are speech channels and said PA is implemented in a speech coder.

17. (New) The Processing Unit (PA) according to claim 13, wherein said process step modules are implemented by means of hardware suitable for the algorithm.

18. (New) The Processing Unit (PA) according to claim 13, wherein at least one of the PS modules transfer data between the external memory and any of the memories within the memory unit.

19. (New) A method for processing a plurality of data streams by an algorithm divided into a plurality of Process Steps (PS) by using an interconnection unit comprising means for switching, Process Step (PS) means comprising at least two PS modules, each connected to the interconnection unit and a scheduler connected to said interconnection unit and to each PS module, said method comprising the steps of:

connecting at least two memories within a memory unit to the interconnection unit;

providing by the interconnection unit a first connection between one of said memories and one of said PS modules and a second connection between another of said memories and another of said PS modules, wherein the interconnection unit is adapted to connect each memory to each of the PS modules by a switching activity, wherein the switching activity and the processing of the PS modules are controlled by the scheduler;

storing a data stream in each memory, and

manipulating said data streams in parallel by the connected PS modules respectively, during a predetermined time period between said switching activities.

20. (New) The method according to claim 19, wherein the method comprises the further step of storing at least input and output data for the memories within the memory unit at the at least one external memory.

21. (New) The method according to claim 19, wherein said data streams are channels in a communication system.

22. (New) The method according to claim 21, wherein said channels are speech channels and that said processing unit is implemented in a speech coder.

23. (New) The method according to claim 19, wherein said process step modules are implemented by means of hardware suitable for the algorithm.

24. (New) The method according to claim 19, wherein at least one of the PS modules transfers data between the external memory and any of the memories within the memory unit.

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